UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,504	04/15/2004	Yuichiro Morita	500.40687CX1	6566

20457 7590 06/25/2008

ANTONELLI, TERRY, STOUT & KRAUS, LLP
1300 NORTH SEVENTEENTH STREET
SUITE 1800
ARLINGTON, VA 22209-3873

EXAMINER	
SAVLA, ARPAN P	

ART UNIT	PAPER NUMBER
2185	

MAIL DATE	DELIVERY MODE
06/25/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/824,504	MORITA ET AL.	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 May 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/12/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on May 12, 2008 has been entered.

Response to Amendment

This Office action is in response to Applicant's communication filed May 12, 2008 in response to the Office action dated February 11, 2008. Claims 1-10 have been canceled. New claims 11-22 have been added. Claims 11-22 are pending in this application.

OBJECTIONS

1. In view of Applicant's amendment, the objections to **claims 3, 5, 8, and 10** are withdrawn.

2. **Claim 15** is objected to because the limitation "a memory control unit operable to read access or write access to an external memory DRAM" should instead read "a memory control unit operable to **have** read access or write access to an external memory DRAM."

3. **Claim 16** is objected to because the limitation "external memory" should instead read "external **DRAM**."

4. **Claim 17** is objected to because the words "access for" should be **deleted**.

5. **Claim 18** is objected to because the limitation "DRRAM" should instead read "DRAM" (i.e. one of the **R**'s should be deleted).

6. **Claim 19** is objected to because the limitation "a memory controller to access **to** an external memory" should instead read "a memory controller to access an external memory" (i.e. the second **to** should be deleted) and the limitation "activate page" in the last line of the claim should instead read "activate**d** page."

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 11-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jones et al. (U.S. Patent 6,233,661) (hereinafter "Jones") in view of Somaya, Deepak and Linden, Greg, "System-on-a-Chip Integration in the Semiconductor Industry: Industry Structure and Firm Strategies" (hereinafter "Somaya").

9. **As per claim 11**, Jones discloses a system comprising:

a central processing unit (col. 5, line 8; Fig. 2, element 102);

and a memory controller for controlling an external memory (col. 7, lines 38-40; col. 8, lines 55-63; Fig. 3, element 140; Fig. 2, element 106),

wherein said memory controller is operable to receive a request for access from said central processing unit to said external memory (col. 9, lines 56-60; Fig. 4A, element 304) having a data storage area divided into a plurality of banks each divided into a plurality of pages (col. 12, lines 35-38; Fig. 4B, element 106),

and wherein said memory controller is operable to activate a page of said external memory to be accessed, based on said access request from said central processing unit, and to execute advance precharge of a page to be accessed subsequently by said central processing unit before accessing said activated page (col. 13, lines 35-39; col. 16, lines 1-15; Fig. 4A, element 308; Figs. 7 and 8).

Jones does not disclose that the system is an LSI.

Somaya discloses a system-on-a-chip (pg. 3). *It should be noted that a Somaya's "system-on-a-chip" is equivalent to Applicant's "LSI."*

Jones and Somaya are analogous art because they are from the same field of endeavor, that being computer systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate Jones' CPU and memory controller as Somaya's system-on-a-chip.

The motivation for doing so would have been to increase operating speeds, lower power consumption, reduce the size and complexity of end-use products, lower unit manufacturing costs, and improve system reliability (Somaya, pg. 4).

Therefore, it would have been obvious to combine Jones and Somaya for the benefit of obtaining the invention as specified in claim 11.

10. **As per claim 15**, Jones discloses a system comprising:

a central processing unit to execute data processing (col. 5, lines 8 and 43-46; Fig. 2, element 102);

a memory control unit operable to have read access or write access to an external DRAM (col. 7, lines 38-40; col. 8, lines 55-63; Fig. 3, element 140; col. 5, lines 53-61; Fig. 2, element 106), *It should be noted that Jones' "memory controller" is equivalent to Applicant's "memory control unit."*

wherein said memory control unit is operable to receive a request for access from said central processing unit to said external DRAM (col. 9, lines 56-60; Fig. 4A, element 304) having a data storage area divided into a plurality of banks each divided into a plurality of pages (col. 12, lines 35-38; Fig. 4B, element 106),

and wherein said memory control unit is operable to activate a page of said external DRAM to be accessed, based on said access request from said central processing unit, and to execute advance precharge of a bank next to be accessed by said central processing unit before accessing said activated page (col. 13, lines 35-39; col. 16, lines 1-15; Fig. 4A, element 308; Figs. 7 and 8).

Jones does not disclose that the system is an LSI.

Somaya discloses a system-on-a-chip (pg. 3). *It should be noted that a Somaya's "system-on-a-chip" is equivalent to Applicant's "LSI."*

Jones and Somaya are analogous art because they are from the same field of endeavor, that being computer systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate Jones' CPU and memory controller as Somaya's system-on-a-chip.

The motivation for doing so would have been to increase operating speeds, lower power consumption, reduce the size and complexity of end-use products, lower unit manufacturing costs, and improve system reliability (Somaya, pg. 4).

Therefore, it would have been obvious to combine Jones and Somaya for the benefit of obtaining the invention as specified in claim 15.

11. **As per claim 19**, Jones discloses a system comprising:

a CPU to execute data processing (col. 5, lines 8 and 43-46; Fig. 2, element 102);

a memory controller to access an external memory synchronized with clock signals (col. 7, lines 38-40; col. 8, lines 55-63; Fig. 3, element 140; col. 5, lines 53-61; Fig. 2, element 106), *It should be noted that an SDRAM is a memory synchronized with clock signals (col. 2, lines 51-56).*

wherein said memory controller is operable to receive a request for access from said CPU to said external memory (col. 9, lines 56-60; Fig. 4A, element 304) having a data storage area divided into a plurality of banks each divided into a plurality of pages, each page being allocated to a bank different from banks to which pages adjacent to said page are allocated (col. 12, lines 35-38; Fig. 4B, element 106),

and wherein said memory is operable to activate a page of a bank to be accessed, based on said access request from said CPU, and to execute advance precharge of a page of the bank to be accessed subsequently by said CPU before accessing said activated page (col. 13, lines 35-39; col. 16, lines 1-15; Fig. 4A, element 308; Figs. 7 and 8).

12. **As per claims 12 and 20**, the combination of Jones/Somaya discloses data of said central processing unit/CPU is stored in said external memory (Jones, col. 5, lines 53-55).

13. **As per claims 13, 16, and 21**, the combination of Jones/Somaya discloses said memory controller/control unit is operable to provide a RAS signal, a CAS signal, a WE signal and an address signal to said external memory/DRAM synchronized with a/said clock signal(s) (Jones, col. 15, lines 16-29; Fig. 6). *It should be noted the "CS (chip select)" is analogous to the "address signal."*

14. **As per claims 14, 18, and 22**, the combination of Jones/Somaya discloses said memory controller/control unit is operable to provide a bank address signal and an address signal to said external memory/DRAM synchronized with a/said clock signal(s) (Jones, col. 15, lines 16-29; Fig. 6). *It should be noted the "bank select" is analogous to the "bank address signal."*

15. **As per claim 17**, the combination of Jones/Somaya discloses said central processing unit is operable to read out an instruction code stored in said external memory (Jones, col. 5, lines 53-55). *It should be noted that "application programs" are analogous to "instruction code."*

Response to Arguments

16. Applicant's arguments with respect to **claims 11-22** have been considered but are moot in view of the new ground of rejection above.

RELEVANT ART CITED BY THE EXAMINER

The following prior art made of record and not relied upon is cited to establish the level of skill in Applicant's art and those arts considered reasonably pertinent to Applicant's disclosure. See MPEP 707.05(e).

1. U.S. Patent 5,872,903 (Iwata et al.) discloses an integrated circuit device with a memory that preserves its content independently of a synchronizing signal when given a self-control request.

2. U.S. Patent 6,226,753 (Arima et al.) discloses a single chip integrated circuit with external bus interface.

3. U.S. Patent 6,247,138 (Tamura et al.) discloses a semiconductor integrated circuit device has a command decoder for issuing a control command in accordance with a supplied control signal, a DRAM core, and a timing adjusting circuit for supplying the control command, set active for a predetermined period, as a DRAM control signal to the DRAM core.

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, **claims 11-22** have received a first action on the merits and are subject of a first action non-final.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571)272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Arpan Savla/
Examiner, Art Unit 2185
June 21, 2008

/Sanjiv Shah/
Supervisory Patent Examiner, Art Unit 2185